

# SEPIANet

## System Embedded Photonics In Access Networks

The project aim was to develop technology solutions for embedded optical architectures in access network head-end systems to allow significant reduction in power consumption, increased energy efficiency, system density and bandwidth scalability, which is currently unfeasible in today's copper driven access network systems.

The SEPIANet project enables up to 1 Gb/s data interconnect to the home while establishing an embedded future-proof interconnect infrastructure allowing further scalability of serial bandwidth to the home up to 10Gb/s in future. To this end a consortium of 5 industrial partners and a world leading research partner drew on their combined expertise in access network system design, glass optical waveguides, electro-optical printed circuit board (EOCB) fabrication, optical PCB interconnect solutions, integrated optical transceiver solutions and high speed VCSEL fabrication to design and develop optical components, modules and subsystems for future access products based on embedded electro-optical printed circuit board technology. Project activities centered on the development of optical printed circuit boards<sup>1</sup> incorporating multimode glass waveguides, lens integrated parallel optical transceiver subassemblies<sup>2</sup>, thermally stable 1310 nm VCSELs and high density pluggable optical connectors<sup>3</sup>. Key outputs from the project included optical devices suitable for direct integration, optical coupling techniques for chip to PCB, optical board-to-board interconnect and pluggable optical PCB connectors, culminating in the production of a demonstration platform<sup>4</sup> showcasing technology solutions developed.

**Funding:** EU piano+  
**Duration:** 1<sup>st</sup> July 2011 – 31<sup>st</sup> of December 2013  
**Website:** <http://www.pianoplus.eu/sepianet.html>

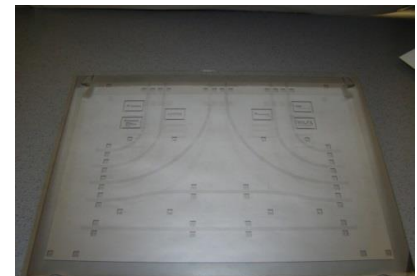


Fig.1 - glass waveguide panel

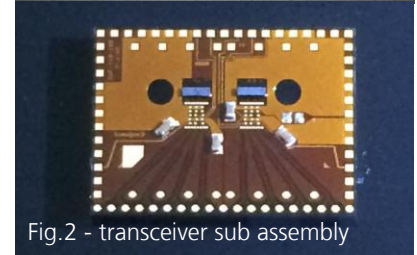


Fig.2 - transceiver sub assembly

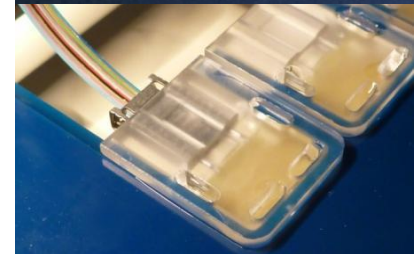


Fig. 3 - optical connector



Fig. 4 - demo platform

